AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a semiconductor layer which contains an element isolation region and adjacent doped layers isolated from each other by the element isolation region; and

a gate connection layer formed over the element isolation region and the adjacent doped layers,

wherein a depth X of the element isolation region and a width Y of the element isolation region satisfy an equation represented by X/Y = 1.33 to 1.67.

2. (Original) The semiconductor device according to Claim 1,

wherein the depth of the element isolation region is in a range of 0.32 to 0.40 μm.

3. (Original) The semiconductor device according to Claim 1,

wherein the element isolation region further comprises a trench element isolation region.

4. (Original) The semiconductor device according to Claim 3,

wherein the element isolation region comprises a trench formed in the semiconductor layer and an insulating layer provided in the trench.

5. (Original) The semiconductor device according to Claim 4,

wherein the insulating layer further comprises an HDP-CVD insulating layer.

6. (Original) The semiconductor device according to Claim 4,

wherein the insulating layer further comprises a TEOS plasma CVD insulating layer.

7. (Original) The semiconductor device according to Claim 4,

wherein the insulating layer further comprises an SOG insulating layer.

8. (Original) The semiconductor device according to Claim 1,

wherein the adjacent doped layers further comprise two doped layers having the same conductivity.

9. (Original) The semiconductor device according to Claim 1,

wherein the adjacent doped layers further comprise two doped layers which have the same conductivity and which are contained in respective memory cells adjacent to each other.

10. (Currently Amended) A semiconductor device comprising:

a semiconductor layer;

adjacent doped layers on the semiconductor layer; ~~and~~

an element isolation region of the substrate isolating the adjacent doped layers from each other; and

a gate connection layer formed over the element isolation region and the adjacent doped layers;

wherein a depth X of the element isolation region and a width Y of the element isolation region satisfy an equation represented by X/Y = 1.33 to 1.67.

11. (Original) The semiconductor device according to Claim 10,

wherein the depth of the element isolation region is in a range of 0.32 to 0.40 μm.

12. (Original) The semiconductor device according to Claim 10,

wherein the element isolation region further comprises a trench element isolation region.

13. (Original) The semiconductor device according to Claim 12,

wherein the element isolation region comprises a trench formed in the semiconductor layer and an insulating layer provided in the trench.

14. (Original) The semiconductor device according to Claim 10,

wherein the adjacent doped layers further comprise two doped layers having the same conductivity.

15. (Original) The semiconductor device according to Claim 10,

wherein the adjacent doped layers further comprise two doped layers which have the same conductivity and which are contained in respective memory cells adjacent to each other.